고급컴퓨터구조

Q1. In virtual memory systems, performance is degraded due to page accesses (twice, at least). How can we reduce the number of page accesses.

Q2. What is cache associativity? What is the relation between associativity and cache hit rate?

Q3. Compared to single cycle implementation, what is the advantage of pipelining? List all the types of hazards and explain them. Additionally, write the solutions to all the types of hazards except stall.

Q4. For I/O operations, there are two methods: polling and interrupt. Explain two methods and present pros and cons of each method.

Q5. Explain RAID(Redundant Array of Inexpensive Disks)

Q6. Explain the feature of RISC processors

Q7. Explain superscalar structure and superpipeline structure.

Q8. Explain cache coherence protocol in multiprocessor systems with an example.

Q9. Explain DMA(Direct Memory Access).

Q10. Why do we need TLB (Translation Lookahead Buffer). In

case of page fault, explain the operation of the TLB?

Q11. What is CPI? In case CPI is low, performance may be higher. But this is not always true; explain this case.

Q12. Explain Amdahl's law. Why is the law related to "make common cases faster"?

Q13. Explain the relation between processor frequency and clock cycle time. Additionally, in case of 2GHz CPU, what is the clock cycle time in terms of ps(pico second)?

Q14. Explain spatial locality AND temporal locality. How do they different? Explain with examples.